Date:

# EXPERIMENT NO. 5

#### AIM: Implement a common bus system with ALU, 8 registers and 1 memory unit

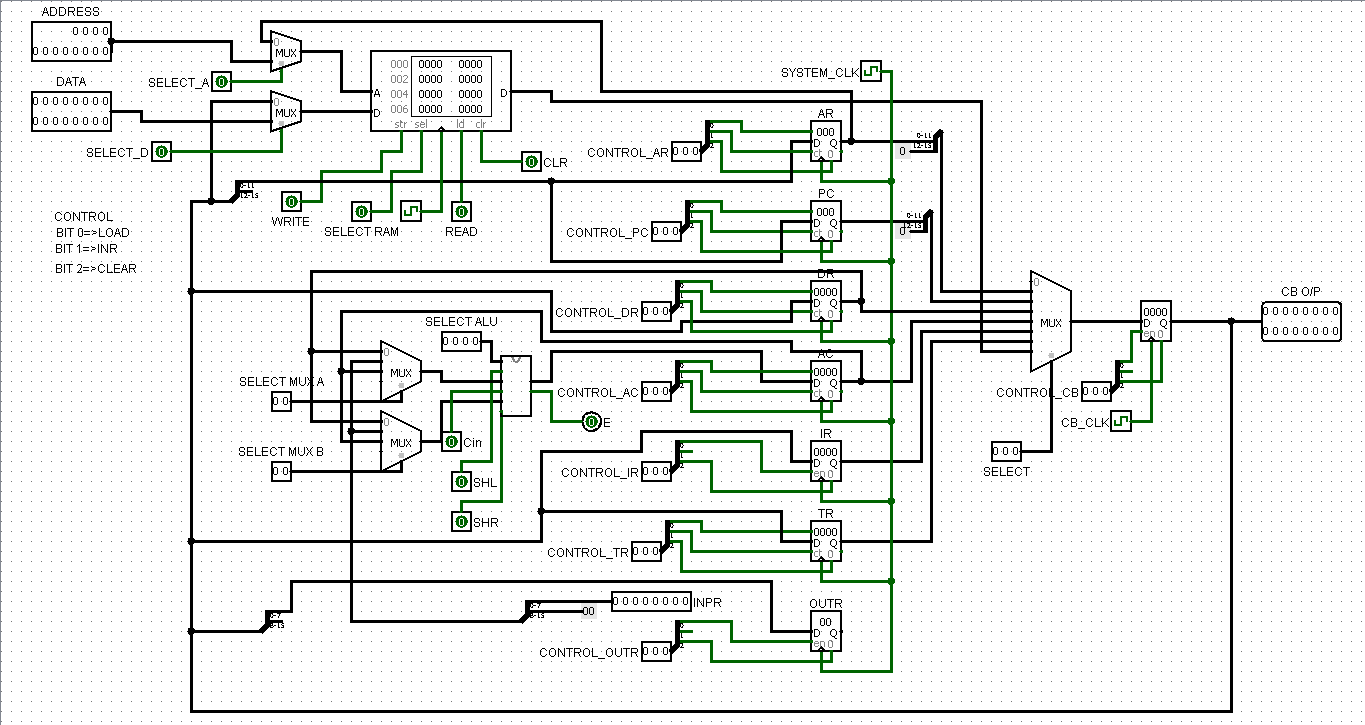
#### with necessary control signals.

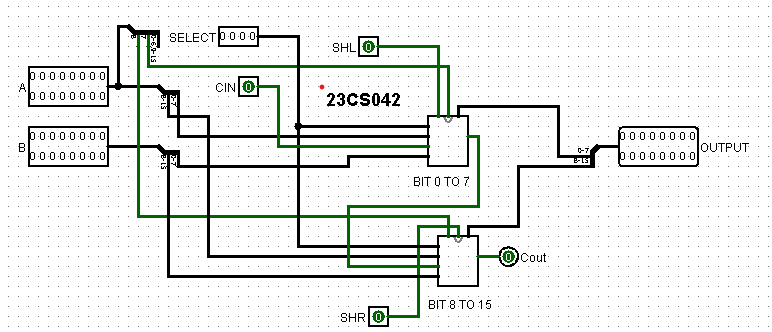
#### OBJECTIVES:

#### Implement 16-bit ALU that is suitable for common bus system

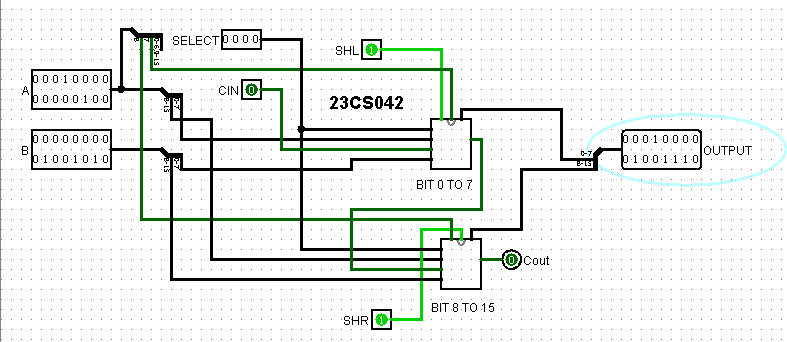
#### Implement 16-bit common bus system with ALU, 8 registers and 1 memory unit

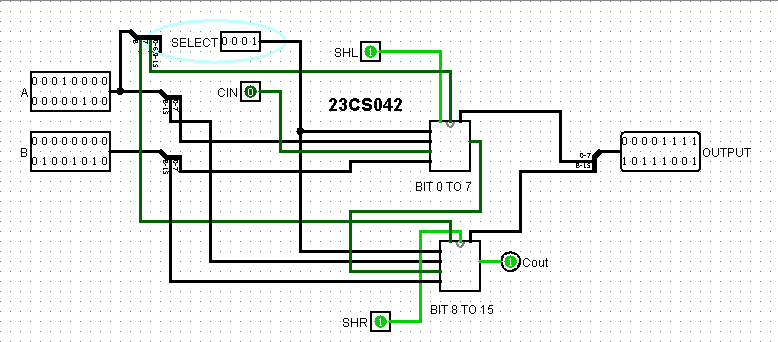
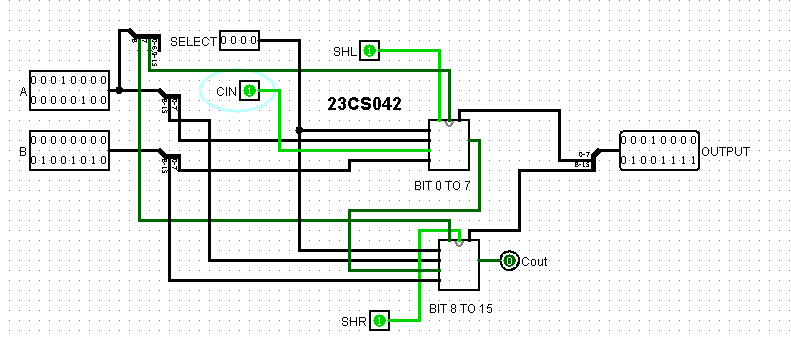
**CIRCUITS:**

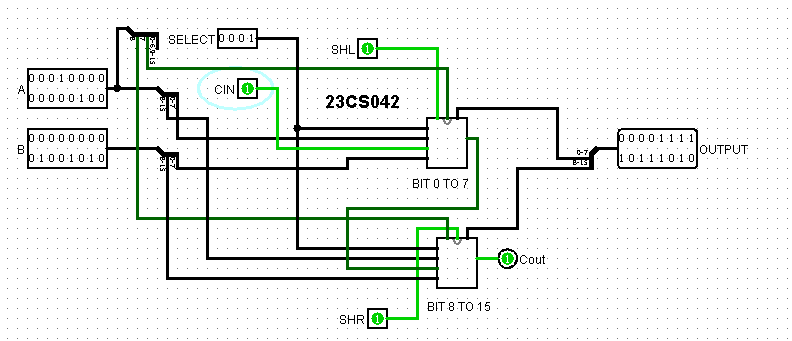


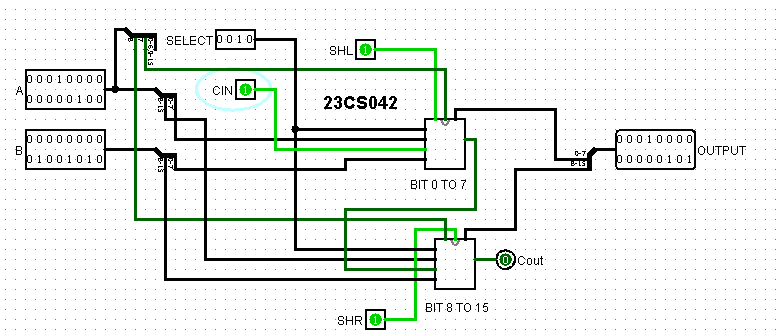
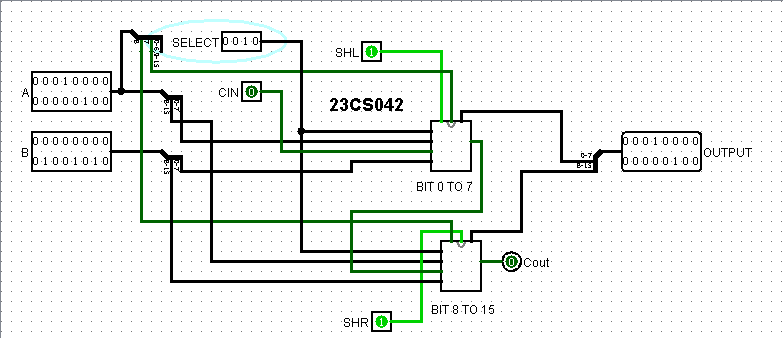


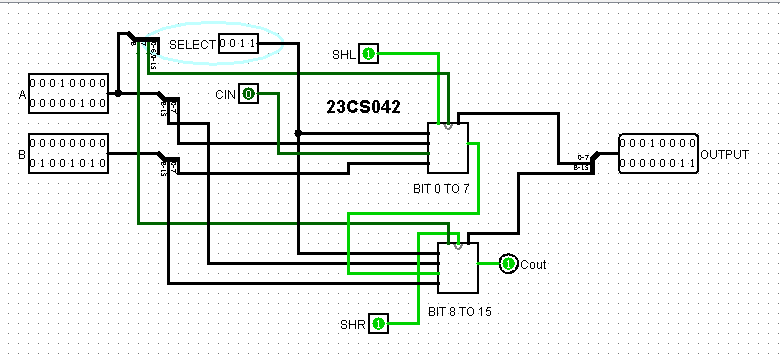
**OUTPUTS:**

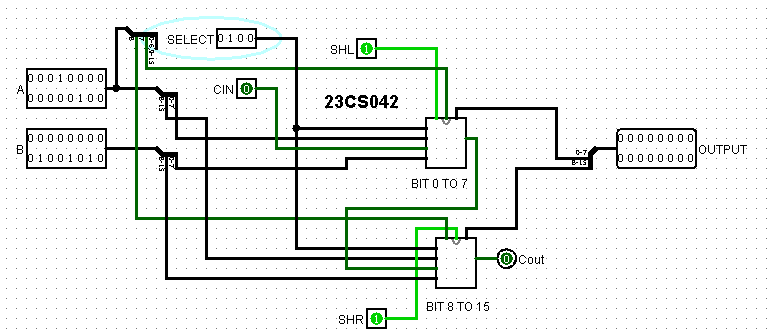
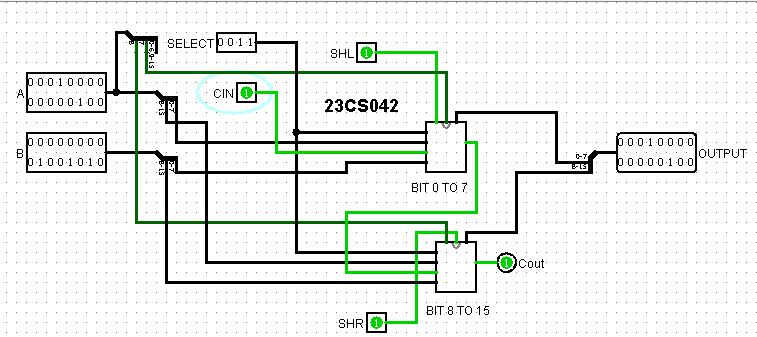


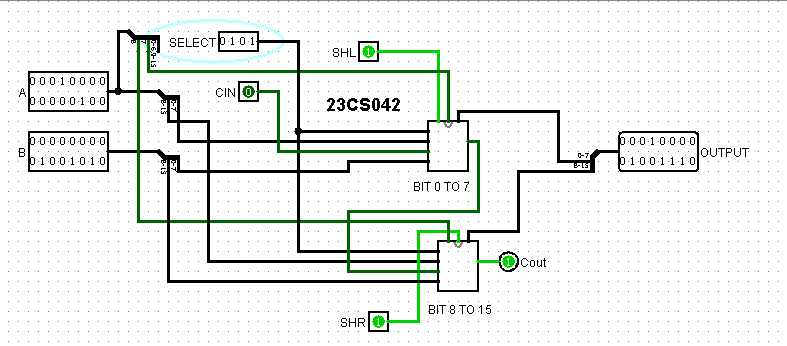


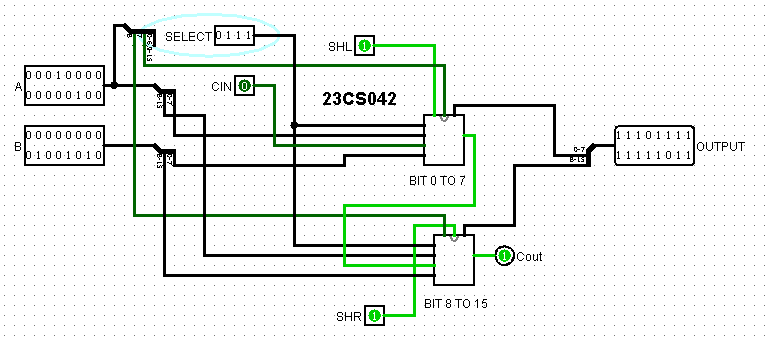
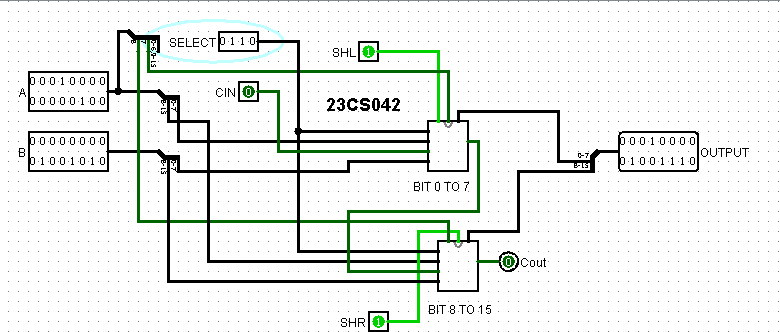


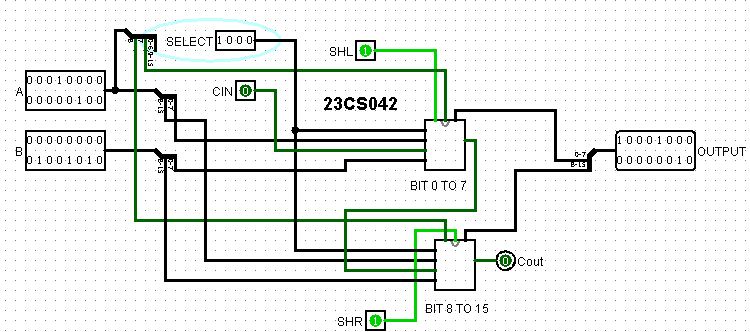


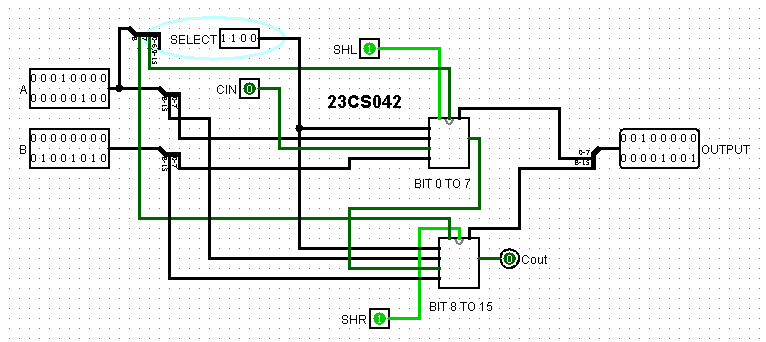




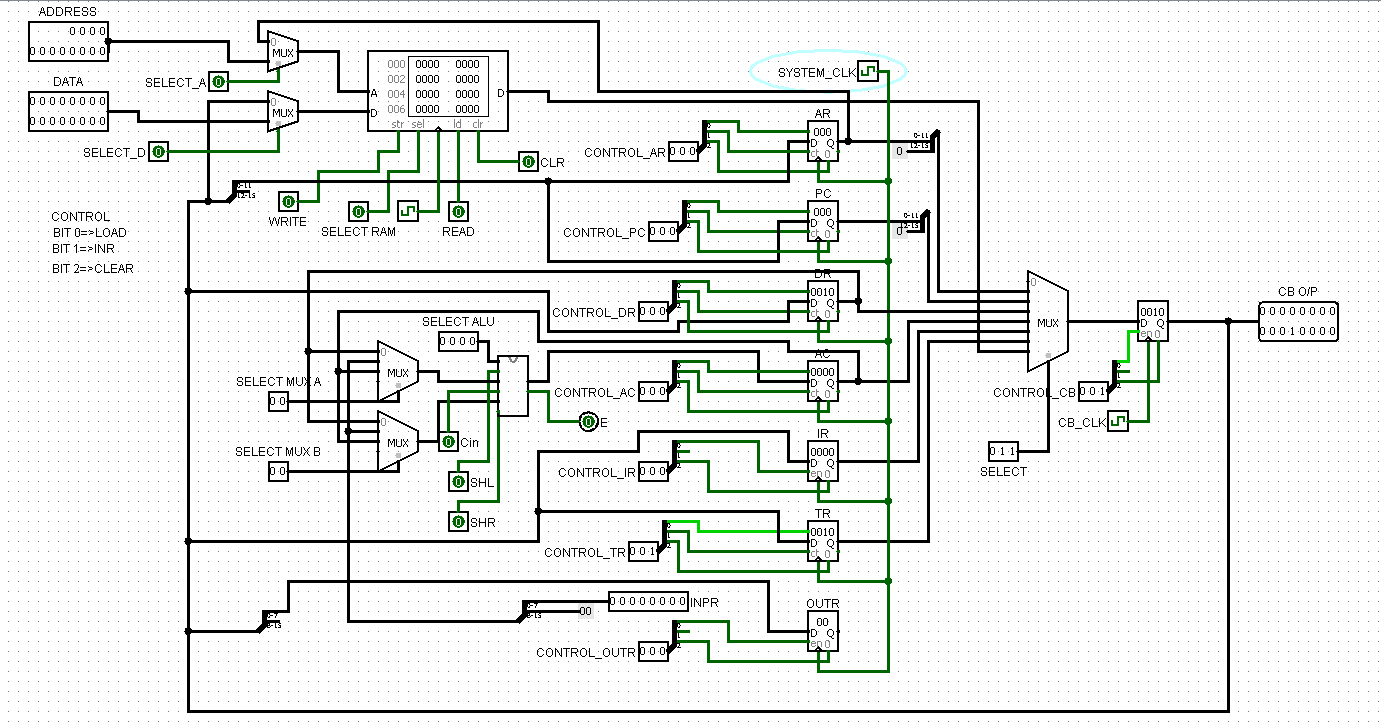




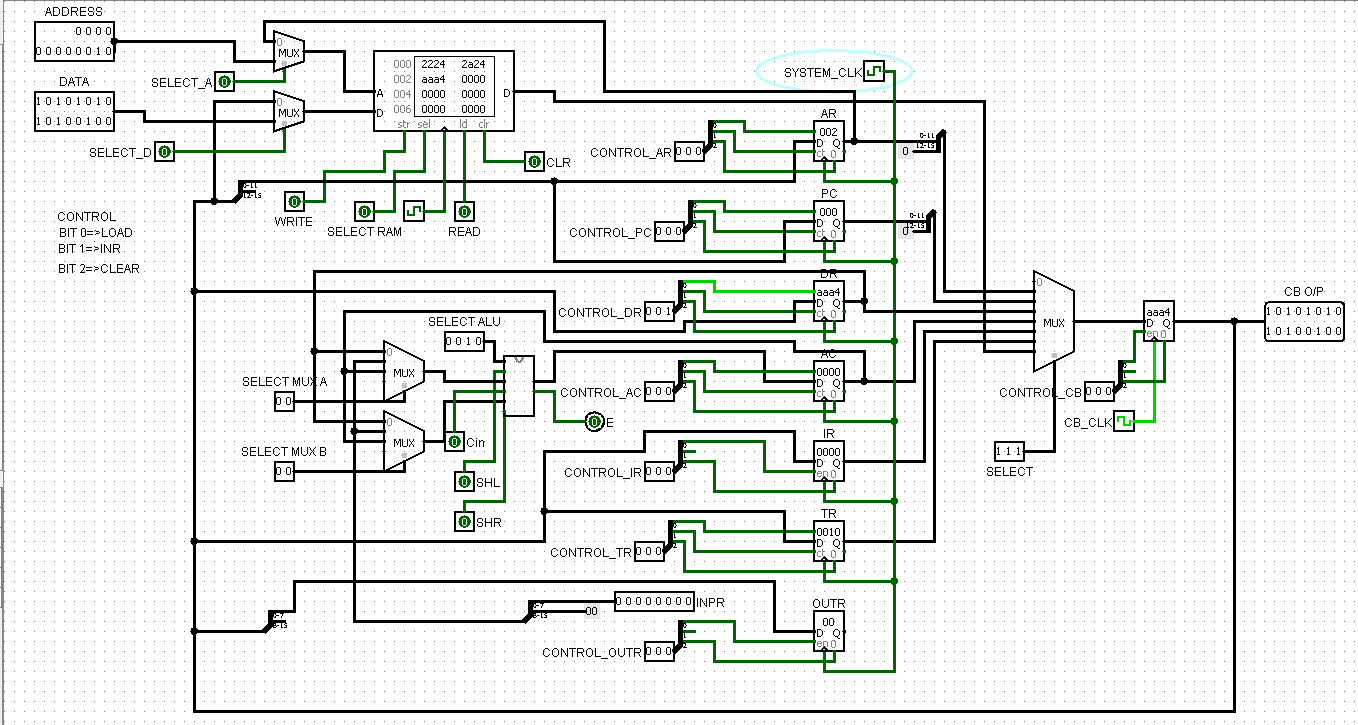




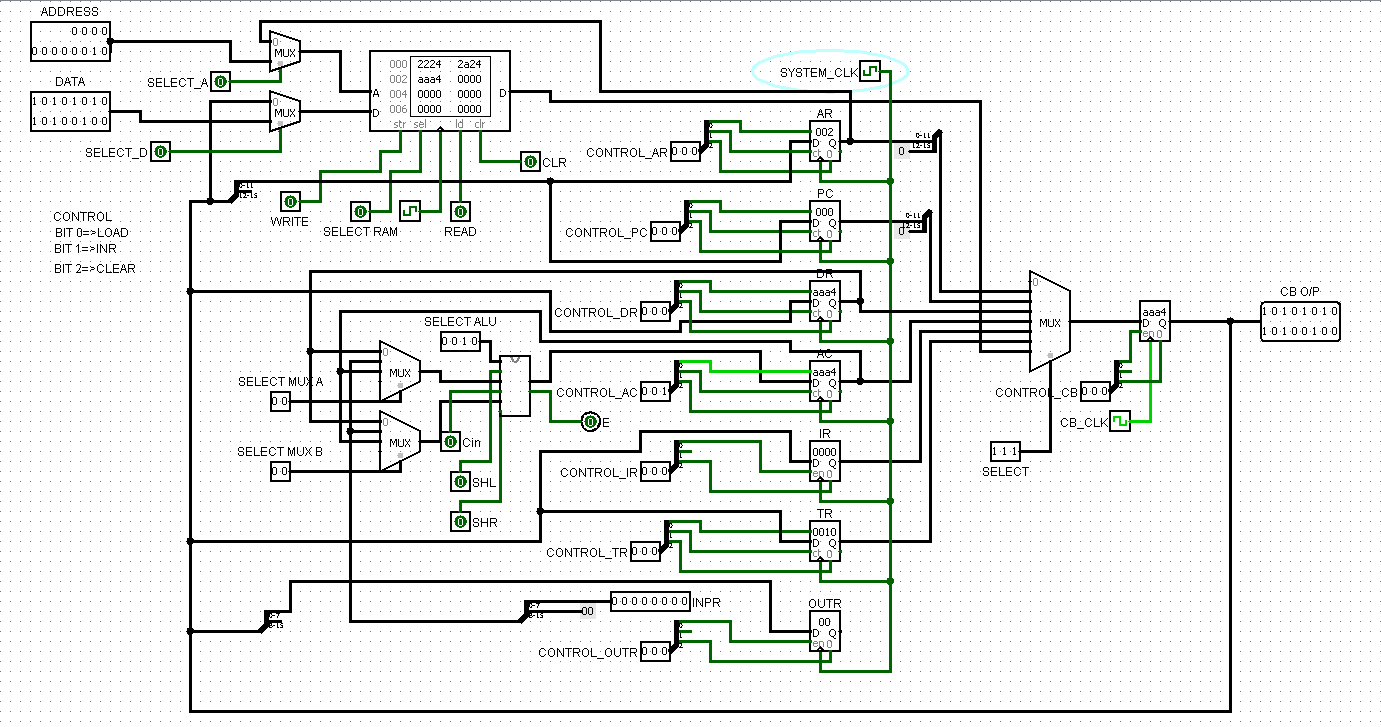
**TR<-DR**



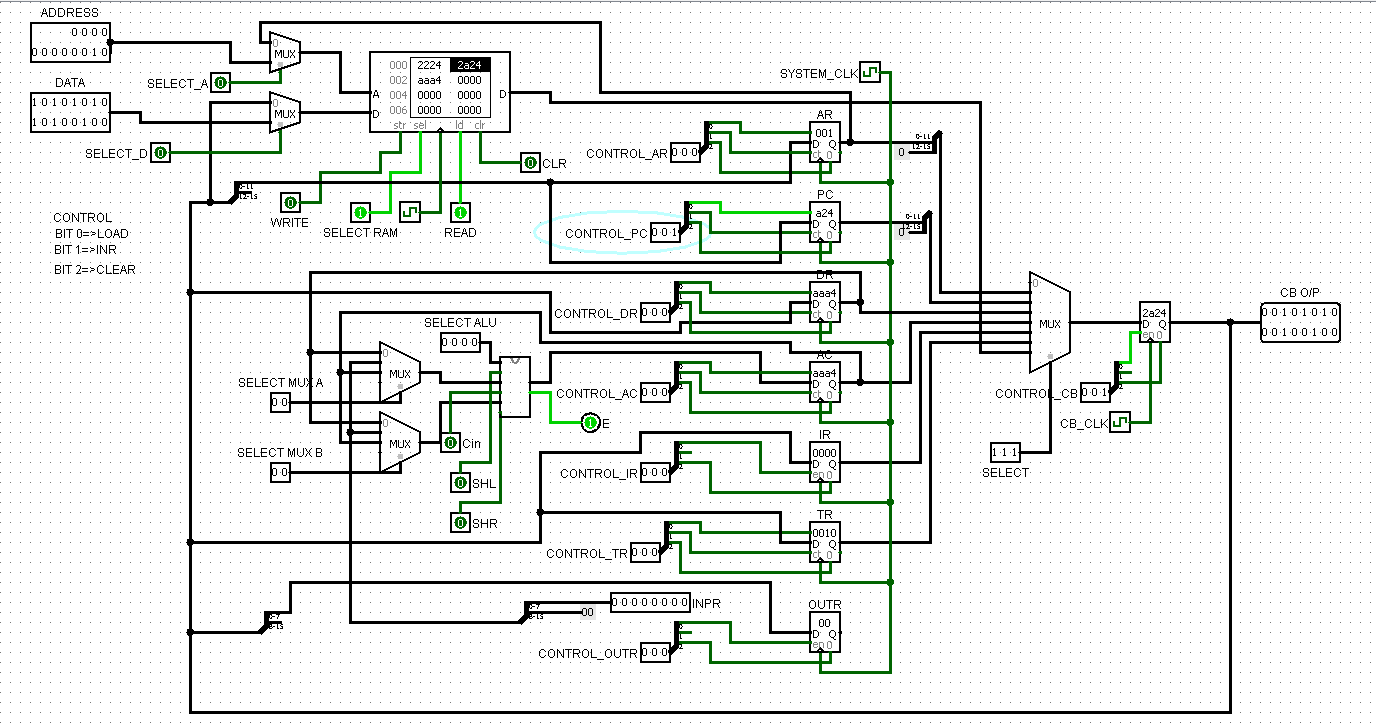
**DR<-MEM[AR]**



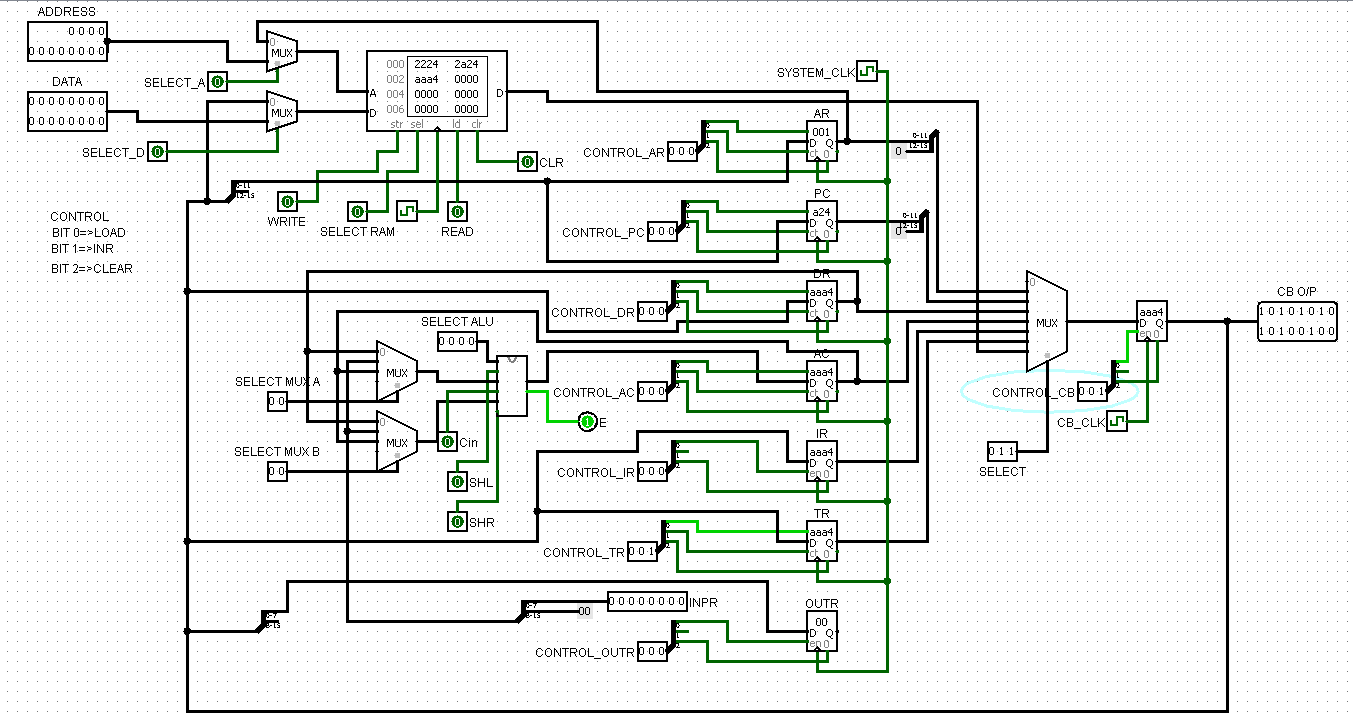
**AC<-DR**



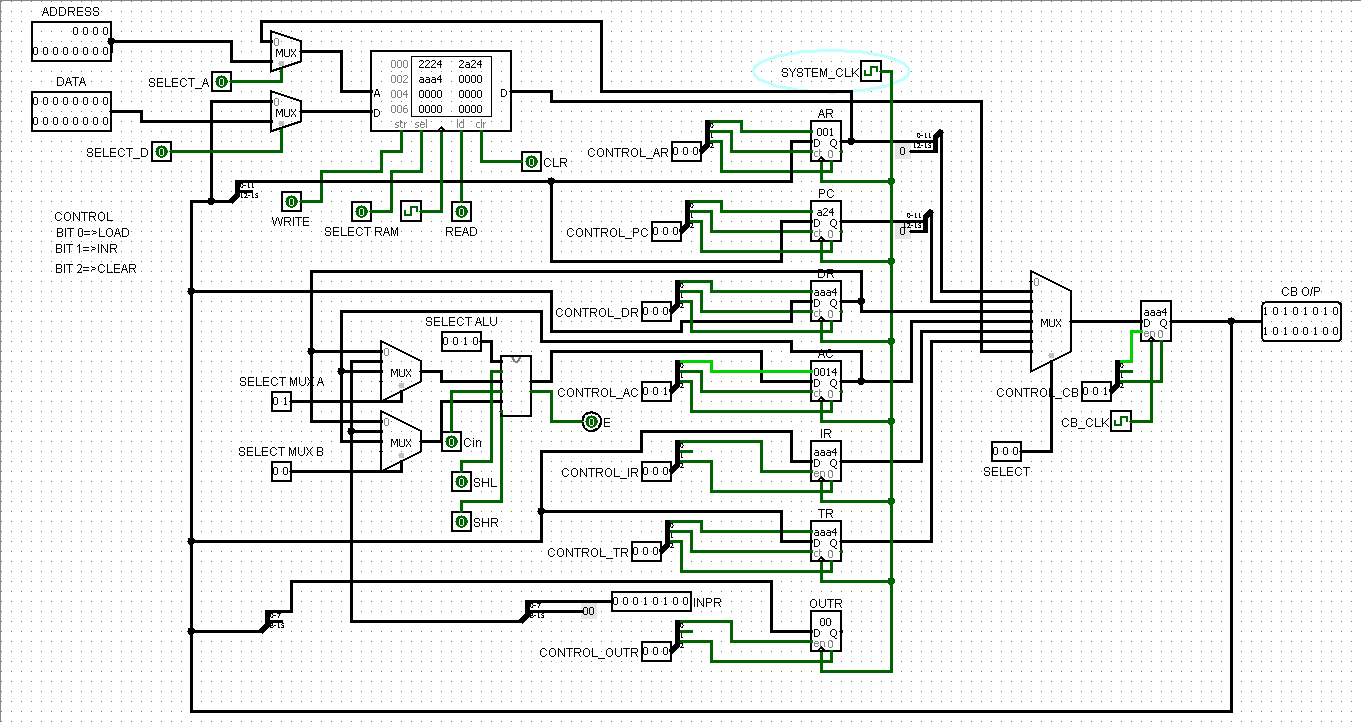
**PC<-MEM[AR]**



**IR<-DR**



**AC<-INPR**



**CONCLUSION:**